SYNC

MODUŁ ODCHYLANIA

2)	CRT00 25/28"
2109	470n
2112	470p
2120	2n2
2129	1n
2428	1µ
2516	100µ
3420	10k
3432	560k
3505	100
3507	1k3
5422	LOT 25/28"

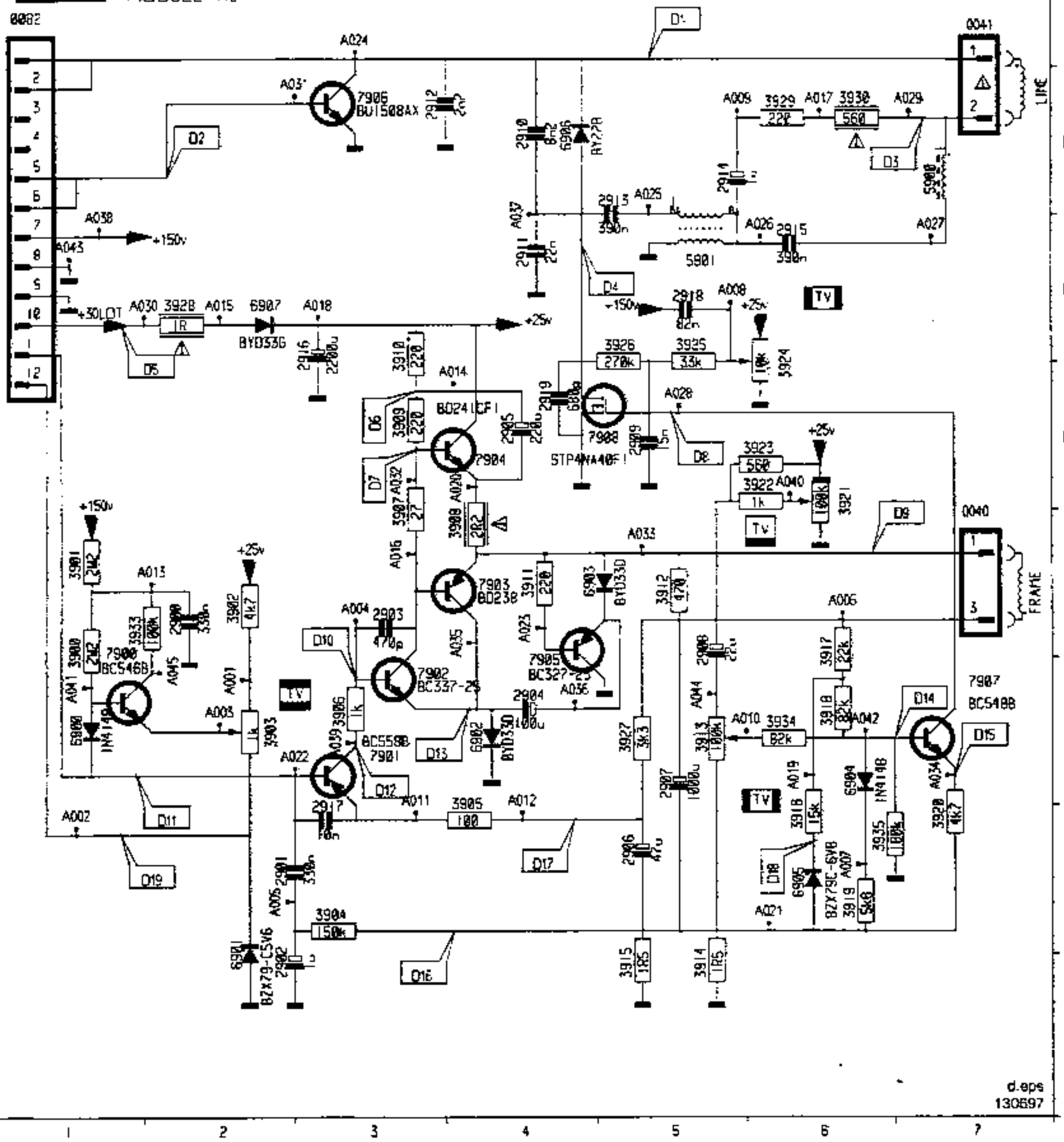
1)	SCA41 PAL	SCA42 PAL/SECAM
7100	TDA8361/N5	TDA8362/N5

4)	CON51 MONO NO TXT	CON53 MONO TXT EUR ETT	CON55 NICAM TXT	CON57 MONO TXT GR/TK
2514	1000µ	2200µ	2200µ	2200µ
3180	--	5k6	5k6	5k6
3433	39k	82k	82k	82k

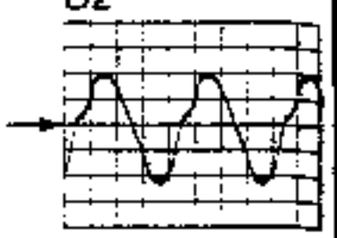
3)	SND02 STEREO 3W	SND81 MONO 3W BGLL'	SND84 MONO 3W NO BGLL'
1503	MP250	MP100	MP100
1504	--	--	--
2512	2200µ	1000µ	1000µ

Rys.2. Schemat ideowy zasilacza i układu odchylania chassis L6.2.

MODULE 110

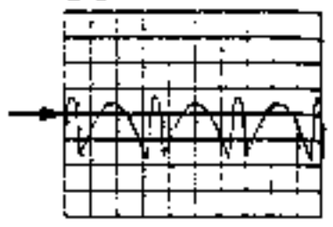


D2



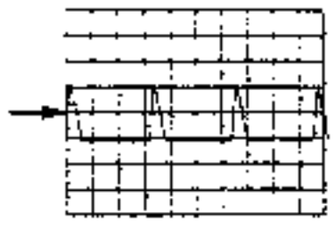
2V / div AC
5ms / div

D3



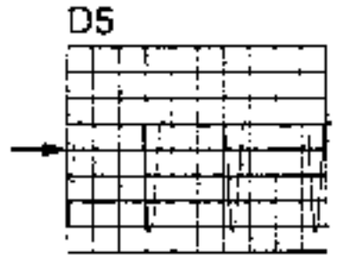
5V / div AC
20µs / div

D4



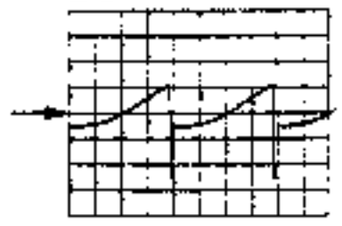
5V / div AC
20µs / div

D5



5V / div AC
20µs / div

D6

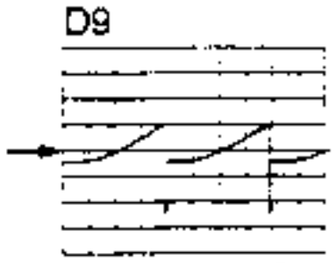


1V / div AC
5ms / div

D7

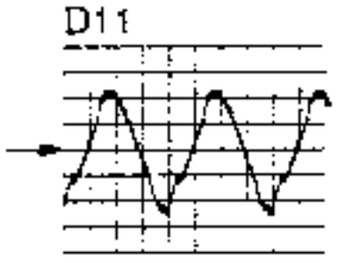
1V / div AC
5ms / div

D9



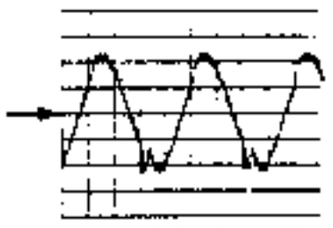
1V / div AC
5ms / div

D11



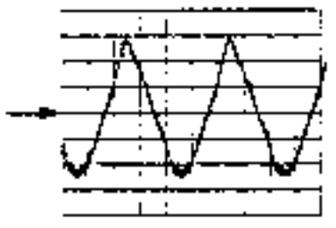
2V / div AC
5ms / div

D13



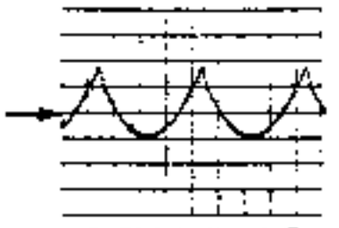
0.5V / div AC
10µs / div

D15



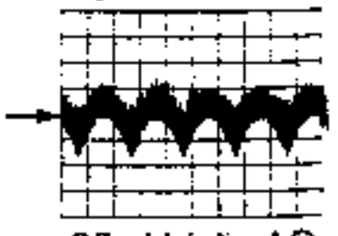
2V / div AC
5ms / div

D17



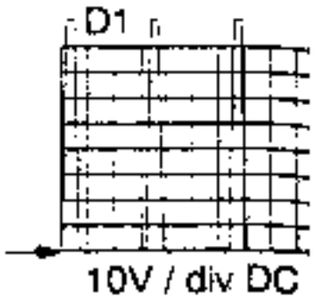
0.2V / div AC
5ms / div

D8



20mV / div AC
10ms / div

D1

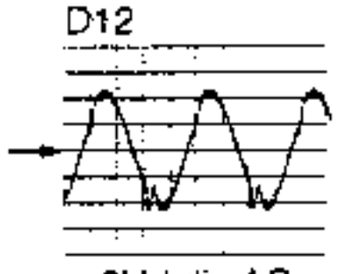


10V / div DC
20µs / div

D10

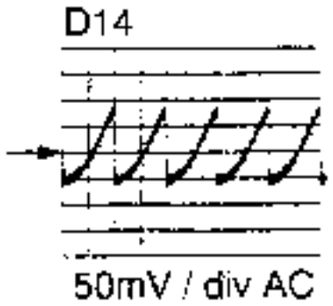
0,5V / div AC
10ms / div

D12



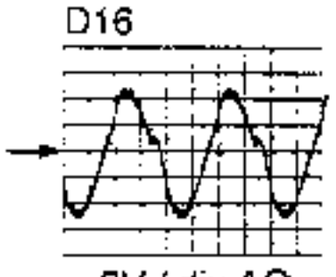
2V / div AC
5ms / div

D14



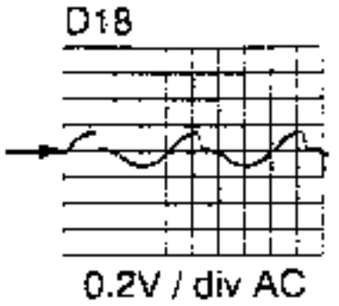
50mV / div AC
10ms / div

D16



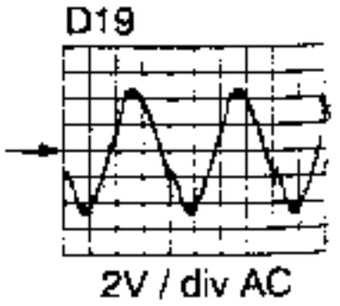
2V / div AC
5ms / div

D18



0.2V / div AC
5ms / div

D19



2V / div AC
5ms / div